WHAT IS CLAIMED IS:

1. A differential phase-locked loop comprising:

a differential detector configured to receive an input signal and a reference signal and to provide a detector output signal indicative of a difference between the input signal and the reference signal;

a differential signal filter coupled to the detector and configured to receive the detector output signal and to provide a control signal; and

a differential voltage controlled oscillator coupled to the signal filter and configured to receive the control signal and to provide an oscillator signal which is adjustable based on the control signal, the oscillator signal is fed back to the detector as the input signal;

wherein the differential detector, the differential signal filter, and the differential voltage controlled oscillator are connected to one another in a fully differential manner.

2. The differential phase-locked loop of claim 1 wherein the differential detector, the differential signal filter, and the differential voltage controller oscillator are each implemented using C^3MOS logic.

3. The differential phase-locked loop of claim 2 further comprising:

a differential Gm cell circuit disposed between the differential detector and the differential signal filter and configured to receive the detector output signal and to provide a current output signal;

wherein the current output signal is fed to the differential signal filter;

wherein the differential Gm cell circuit is coupled to the differential detector and the differential signal filter in a fully differential manner; and

wherein the differential Gm cell circuit is implemented using C^3MOS logic.

4. The differential phase-locked loop of claim 2 further comprising:

a differential divider circuit disposed between the differential voltage controlled oscillator and the differential detector;

wherein the differential divider circuit is coupled to the differential voltage controlled oscillator and the differential detector in a fully differential manner; and

wherein the differential divider circuit is implemented using C^3MOS logic.

5. The differential phase-locked loop of claim 1 wherein the differential detector is a differential phase-frequency detector.

6. The differential phase-locked loop of claim 1 wherein the differential signal filter is a differential lowpass filter.

7. The differential phase-locked loop of claim 1 wherein the input signal, the reference signal, the detector output signal, the current output signal, the control signal and the oscillator signal are implemented in a differential manner.

8. The differential phase-locked loop of claim 1 wherein the differential detector further includes:

first and second resetable flip-flops configured to receive a first and a second differential signal respectively;

an AND logic function configured to receive differential outputs from the first and second resetable flip-flops; and

one or more buffers configured to receive output from said AND logic function and to provide a reset signal to reset the first and second resetable flip-flops.

9. An integrated circuit comprising the differential phase-locked loop of claim 1.

10. A communication system comprising the differential phase- locked loop of claim 1.

11. A phase-locked loop comprising:

a detector configured to receive a differential input signal and a differential reference signal and to provide a differential detector output signal indicative of a difference between the differential input signal and the differential reference signal;

a Gm cell circuit coupled to the detector and configured to receive the differential detector output signal and to provide a differential current output signal;

a signal filter coupled to the Gm cell circuit and configured to receive the differential current output signal and to provide a differential control signal; and

a voltage controlled oscillator coupled to the signal filter and configured to receive the differential control signal and to provide a differential oscillator signal which is adjustable based on the differential control signal, the differential oscillator signal is fed back to the detector as the differential input signal;

wherein the detector, the GM cell circuit, the signal filter, and the voltage controlled oscillator are each implemented using C^3MOS logic.

12. The phase-locked loop of claim 11 further comprising:

a divider circuit disposed between the voltage controlled oscillator and the detector;

wherein the divider circuit is configured to receive the differential oscillator signal and to provide a differential divided signal to be fed to the detector as the differential input signal; and

wherein the divider circuit is implemented using C^3MOS logic.

13. The phase-locked loop of claim 11 wherein the detector is a phase-frequency detector.

14. The phase-locked loop of claim 11 wherein the signal filter is a lowpass filter.

15. The phase-locked loop of claim 11 wherein the detector further includes:

first and second resetable flip-flops configured to receive a first and a second differential signal respectively;

an AND logic function configured to receive differential outputs from the first and second resetable flip-flops; and

one or more buffers configured to receive output from said AND logic function and to provide a reset signal to reset the first and second resetable flip-flops.

16. An integrated circuit comprising the phase-locked loop of claim 11.

17. A communication system comprising the phase-locked loop of claim 11.

18. A phase-locked loop comprising:

a detector configured to receive an input signal and a reference signal and to provide a detector output signal indicative of a difference between the input signal and the reference signal;

a Gm cell circuit coupled to the detector and configured to receive the detector output signal and to provide a current output signal;

a signal filter coupled to the Gm cell circuit and configured to receive the current output signal and to provide a control signal;

a voltage controlled oscillator coupled to the signal filter and configured to receive the control signal and to provide an oscillator signal which is adjustable based on the control signal; and

a divider circuit coupled to the voltage controlled oscillator and configured to receive the oscillator signal and to provide a divided version of the oscillator signal to be fed to the detector as the input signal;

wherein the detector, the Gm cell circuit, the signal filter, the voltage controlled oscillator and the divider circuit are connected to one another in a fully differential manner; and

wherein the detector, the Gm cell circuit, the signal filter, the voltage controlled oscillator and the divider circuit are implemented using C^3MOS logic.

19. The phase-locked loop of claim 18 wherein the differential detector further includes:

first and second resetable flip-flops configured to receive a first and a second differential signal respectively;

an AND logic function configured to receive differential outputs from the first and second resetable flip-flops; and

at least one buffer configured to receive differential output from the AND logic function and to provide a reset signal to reset the first and second resemble flip-flops.

20. A method for implementing a phase-locked loop having a plurality of components including a detector, a signal filter, a voltage controlled oscillator and a divider circuit, comprising:

connecting each of said plurality of components to one another in a differential manner; and

implementing each of said plurality of components using C^3MOS logic.

21. A method for implementing a phase-locked loop, comprising:

providing a differential input signal and a differential reference signal to a detector;

providing a differential detector output signal from the detector as input to a signal filter;

providing a differential control signal from the signal filter as input to a voltage controlled oscillator; and

providing a differential oscillator signal from the voltage controlled oscillator as the input signal to the detector.

22. The method of claim 21 further comprising:

implementing the detector, the signal filter and the voltage controlled oscillator using C^3MOS logic.

23. The method of claim 21 further comprising:

disposing a Gm cell circuit between the detector and the signal filter;

providing the differential detector output signal from the detector as input to the Gm cell circuit; and

providing a differential current output signal from the Gm cell circuit as input to the signal filter.

24. The method of claim 23 further comprising:

implementing the Gm cell circuit using C^3MOS logic.

25. The method of claim 21 further comprising:

disposing a divider circuit between the voltage controlled oscillator and the detector;

providing the differential oscillator signal from the voltage controlled oscillator as input to the divider circuit; and

providing a divided version of the differential oscillator signal from the divider circuit as the differential input signal to the detector.

26. The method of claim 25 further comprising:

implementing the divider circuit using C^3MOS logic.

27. A method for implementing a phase-locked loop, comprising:

providing a differential input signal and a differential reference signal to a detector;

providing a differential detector output signal from the detector as input to a Gm cell circuit;

providing a differential current output signal from the Gm cell circuit as input to a signal filter;

providing a differential control signal from the signal filter as input to a voltage controlled oscillator;

providing a differential oscillator signal from the voltage controlled oscillator as input to a divider circuit;

providing a divided version of the differential oscillator signal from the divider circuit as the differential input signal to the detector; and

implementing the detector, the Gm cell circuit, the signal filter, the voltage controlled oscillator and the divider circuit using C^3MOS logic.